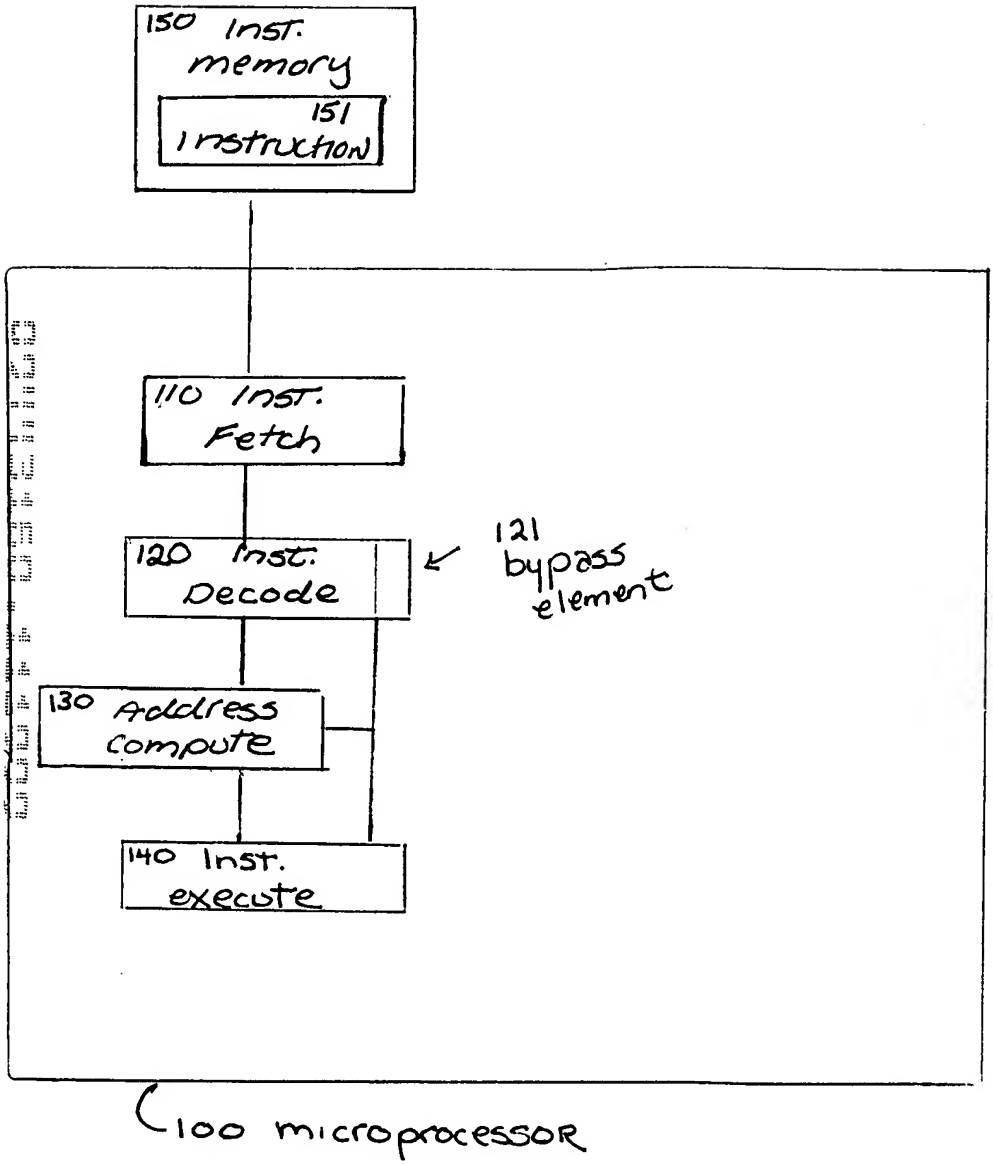
150 Inst. memory
151 Instruction
110 Inst. Fetch
120 Inst. Decode
121 bypass element
130 Address compute
140 Inst. execute
100 microprocessor

210
Microprocessor is coupled to an instruction memory 150 which includes a plurality of instructions 151, and is ready to perform those instructions 151.

211
The microprocessor reads a sequence of instructions 151 from the memory 150 using instruction fetch stage 110.

212
Instruction fetch stage 110 couples the instructions 151 to the instruction decode stage 120.

213(a)
The instruction decode stage 120 parses the instructions 151 to determine whether they are instructions to load data to an external memory or store data from an external memory.

213(b)
The instruction decode stages 120 determines the syntax of any addresses in the external memory that the instructions 151 refer to as operands.

214
The bypass element 121 examines parts of the instruction 151, including information about what operations the instructions 151 command the microprocessor 100 to perform. If these operations are to load or store data, the method continues with step 115. If these operations are otherwise, the method continues with step 221.

215
A record of the symbolic operands of the store operations to external memory is stored in a table that is indexed by the instruction ID.

216
Each load instructions' operands are compared against the store instructions being issued in the ongoing clock cycle and those of all unretired store instructions.

217
The bypass element 121 determines whether the operand addresses that the instructions 151 refer to include identical base address values. If so, the bypass element generates a bypass signal. If not, the bypass element does not generate a bypass signal.

220
The microprocessor can act on the knowledge that the instructions 151 refer to identical locations in an external memory.

221
The instruction decode stage 120 couples the parts of the instruction 151, including information about the base address value and the offset address value to the address computation stage.

TO FIG 2B

FROM FIG. 2A

222
The address computation stage receives the base address value and the offset address value and computes the effective reference address of the instruction 151.

223
The instruction decode stage 120 couples the parts of the instruction 151 to the instruction execution stage 140.

224
The address computation stage 130 couples the effective reference address of the instruction 151 to the instruction execution stage 140.

225
The first (store) instruction is physically performed and completed by external memory.

226(a)
If the bypass signal was generated, the microprocessor proceeds without performing the second load instruction 151. If the bypass signal was not generated then the method proceeds at step 226(b.)

226(b)
If the bypass signal was not generated (or if an inverse bypass signal was generated), the second load instruction 151 is physically performed and completed by external memory.